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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
ITL.0552US

In Re Application Of: **Nathan Y. Moyal**

Serial No.	Filing Date	Examiner	Group Art Unit
09/966,481	**September 28, 2001**	**Hai L. Nguyen**	**2816**

Invention: **Generating Pulses for Resetting Integrated Circuits**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **January 20, 2004**

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Signature

Dated: **March 17, 2004**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	NATHAN Y. MOYAL	§	Group Art Unit:	2816
Serial No.:	09/966,481	§	Examiner:	Hai L. Nguyen
Filed:	September 28, 2001	§		
For:	GENERATING PULSES FOR RESETTING INTEGRATED CIRCUITS	§	Atty. Dkt. No.:	INTL-0552-US (P11111)

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APPEAL BRIEF

Sir:

Applicant respectfully appeals from the final rejection mailed October 24, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 012458/0698.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF THE CLAIMS

The application was originally filed with claims 1-30. Claims 11-13, 16-18, 20 and 44-46 are pending. Claims 11-13, 16-18, 20 and 44-46 are the subject of this appeal.

Date of Deposit: March 17, 2004
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Jennifer Juarez

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF THE INVENTION

Referring to Figure 1, a functional block F may be controlled by a power-on reset circuit 10 to prevent its release for normal operation prior to the time that both a power supply has stabilized and the logic in the functional block F has transitioned to predetermined logic states. The power-on reset circuit 10, in one embodiment, may include the decision logic 12, a latch 14, a pulse generator 16, and an amplifier 18a that couples a signal feedback 20 back to the functional block F. The circuit 10 may be integrated on the same chip as the block F in one embodiment. The functional block F may generate a plurality of output signals I_0 through I_N. Each of the signals is received by the decision logic 12 so that the decision logic 12 can determine whether the logic of the functional block F is in the proper predetermined, initial states to begin normal operation. See Specification, p. 3.

During start-up, the signals I_0 through I_N may be in some random state where it is highly probable that at least some of these signals are high and some are low. The decision logic 12 yields a low output to the S node of the latch 14 if one or more of the outputs I_O to I_N of the functional block F is not in its predetermined state. The decision logic tests the signals I_O to I_N to determine whether those signals are in their proper initial states.

Meanwhile, the pulse generator 16 initially generates a high pulse into the R node of the latch 14 when the supply voltage is ramping up. The combination of a low S node and high R node may result in a reset signal being sent to the functional block F through the amplifier 18a and the signal feedback 20. Thus, the pulse generator 16 may trigger the latch 14 to generate the reset signal to place the logic in the functional block into correct initial states.

The reset signal resets the logic in the functional block F to a desired predetermined state. As a result, the outputs I_0 through I_N yield known good states. When these good states are detected by the decision logic 12, this results in the latch 14 node S going high. The reset signal remains active until the node S has become high, indicating that the functional block's logic is ready, and the pulse generator 16 signal has gone away, indicating that the power supply is now fully operational.

When the pulse generator 16 signal is gone and logic indicates ready (S node = 1), normal chip operation begins in the functional block F. If the logic in the functional block F is not ready, for example due to long routing or for some other reason, the reset remains active, preventing normal operation of the function block F. See Specification, pp. 3-4.

Referring, next to Figure 2, the functional block F in this example is a counter having logic in the form of a plurality of flops only a few of which are shown. The reset signal (on feedback 20) to the flops is generated as soon as the pulse generator 16 is activated. The reset signal is active regardless of the indication from the logic within the functional block F. This is a desirable property because during start-up it is possible to have faulty indicators from the functional block F. See Specification, p. 5.

Referring to Figures 3a through 3c, the power supply signal Vcc shown in Figure 3a ramps up at 22 (when turned on) to a Vcc level 24. During the ramping (at 22), as shown in Figure 3b, the pulse generator 16 signal undergoes the transition to the high level 26 causing the functional block logic to go to "ready" (S=1), as indicated at 30 in Figure 3c. When the pulse generator 16 signal is high (Figure 3b) the logic AND is high (Figure 3c), the pulse generator 16 signal goes low (R=0) as indicated at 28 in Figure 3b. The pulse generator 16 signal being low causes the reset signal to go low releasing the logic in the functional block F, as indicated at 32

in Figure 3c. Logic glitches, indicated at 34 and 36, do not reactivate the reset signal, in one embodiment of the present invention, due to the latching action.

In the event that the I_0 through I_N AND signals indicate a high prior to the pulse generator 16 signal high 26, as indicated in Figures 4b and 4c, the circuit 10 still functions correctly in one embodiment. For example, as shown in Figure 4a, during the ramp indicated at 22, the pulse generator 16 signal goes high as indicated at 26 in Figure 4b. Since the pulse generator 16 signal is high and the logic AND is high, the pulse generator 16 signal goes low as indicated at 28. The reset low results, causing the logic to release. Again logic glitches indicated at 34 and 36 do not reactivate the reset signal. See Specification, pp. 6-7

Referring to Figure 5, in accordance with one embodiment of the present invention, a particular pulse generator 16 is described. The pulse generator 16 shown in Figure 5 includes activation circuits 40 that handle the feedback of the output pulse from pulse generator 16 along the line 55. In particular, the activation circuits 40 receive the feedback of the output pulse so that, once the pulse generator 16 signal goes away, the pulse generator 16 is not inadvertently reactivated. The activation circuits 40 may also ensure that a predetermined supply voltage level is achieved before beginning the power-on reset pulse generator 16 operation in one embodiment. The activation circuits 40 provide outputs 53a and 53b to the capacitor circuits 44. See Specification, pp. 7-8.

After the supply voltage has reached its designated output level for the desired time period, the output 47a is high and the output 47b is low in one embodiment. These signals are conveyed to the hysteresis sense stages 48a and 48b. The output of the hysteresis sense stage 48a may be coupled to a logic functionality 52.

The logic functionality 52 determines whether the signal is at an appropriate level to accurately trigger the logic in the functional blocks being initialized. While a variety of different techniques may be utilized for testing the output of one or more hysteresis sense stages 48, in one embodiment, the most difficult logic to trigger may be emulated in the logic functionality 52. In some embodiments, the toughest logic is an inverter-like stage with stacked p-channel transistors because such a stage has particularly poor headroom.

If the power supply voltage level is too low, the decision logic 54 yields a pulse that may be applied as indicated in Figure 1 for example. The decision logic 54 receives signals from the hysteresis sense stages 48a and 48b. The decision logic 54 generates a high pulse if the ground connected capacitor 64 did not charge up to Vcc or the power connected capacitor 56 did not charge up to Vss or the functional logic 52 did not pass the signal. The pulse generator 16 continues during the power supply ramp up. When that ramp up is over for a sufficient period of time, the decision logic 54 causes the pulse generator 16 output to go away. See Specification, pp. 9-10.

VI. ISSUES

A. Are Claims 11, 13, 16-18, 20, 44 and 45 Patentable Under 35 U.S.C. §102(b) Over Shay?

B. Is Claim 12 Patentable Under 35 U.S.C. §103(a) Over Shay in View of Ansel?

C. Is Claim 46 Patentable Under 35 U.S.C. §103(a) Over Shay in View of Wu?

VII. GROUPING OF THE CLAIMS

For purposes of this appeal, the claims do not stand or fall together. Instead, for purposes of this appeal claims 11, 13, 16-18, 20, 44 and 45 may be grouped together, as set forth above, and claim 12 and claim 46 stand alone.

VIII. ARGUMENT

A. Claims 11, 13, 16-18, 20, 44 and 45 Are Patentable Under 35 U.S.C. §102(b) Over Shay

Independent claim 11 is directed to an integrated circuit that includes an activation circuit, a pulse generator, and a feedback path to provide an output pulse of the pulse generator to the activation circuit. More particularly, the recited pulse generator is to generate output pulses to indicate that a supply voltage is ramping up and to terminate the generation of the pulses after the supply voltage reaches a predetermined level. Claim 11 stands rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,323,067 ("Shay"). Shay fails to disclose a pulse generator that operates in a manner defined by claim 11, and thus the rejection is improper.

The Examiner relies on transistors 68, 70, 72 and 74 of FIG. 1 of Shay to meet such a pulse generator. The operation of those transistors is described in Shay's Detailed Description at col. 4, line 16 through col. 5, line 33. The Examiner asserts that the above-referenced portion of Shay discloses a pulse generator that generates pulses to indicate that a power supply is ramping up, and to terminate the generation of pulses after the supply voltage reaches a predetermined level. Final Office Action, p. 3. However, the Examiner seriously misapprehends the subject matter disclosed by Shay, and Shay fails to provide a sustainable basis for rejection of claim 11.

Specifically, a rejection of a claim under 35 U.S.C. §102(b) requires that a prior art reference disclose expressly or inherently every limitation contained in the claim. *Rowe v. Dror*, 42 U.S.P.Q.2d 1550 (Fed. Cir. 1997). If any claimed element is absent from the reference, there

is no anticipation. *Id.* A prior art reference must disclose each claimed element clearly enough to prove its existence in the prior art. *Motorola, Inc. v. Inter-digital Tech. Corp.*, 43 U.S.P.Q.2d 1481 (Fed. Cir. 1997). Such proof is lacking here.

In this regard, there is no disclosure in Shay that the group of transistors relied upon by the Examiner operates as a pulse generator in the manner required by claim 11. Shay itself refers to these devices as constituents of a latch 18. Shay also indicates that transistors 68, 70, 72, and 74 form an inverter. *See* Shay at col. 3, lines 56-68. It may not be plausibly maintained that a skilled artisan would equate Shay's latch or inverter to the claimed pulse generator. Instead, Shay discloses to the skilled artisan a structure and an associated function that are markedly different than a pulse generator, much less a pulse generator that operates in the specific manner of claim 11.

Furthermore, it is clear from Shay that the voltage at node 38 of FIG. 1 of Shay (which is relied on by the Examiner to anticipate ramping up and termination of pulses), bears no resemblance to the output of the claimed pulse generator. In this regard, Shay's V_{38} goes positive when the supply voltage surpasses a predetermined threshold. Rather than returning to its initial value after a time interval, V_{38} remains high. In fact, due to the operation of latching transistor 76, V_{38} remains high even in the face of transient negative excursions in the supply voltage. Shay, col. 6, lns. 5-12. Thus no reasonable, objective construction of Shay can possibly meet the pulse generator of claim 11.

Moreover, the Final Office action fails to provide any explanation of the manner in which Shay allegedly discloses a pulse generator that operates in the manner recited by claim 11. Conclusory statements, unaccompanied by any reasoning that supports a conclusion of unpatentability, do not satisfy statutory requirements imposed by well-settled patent law. *In re*

Lee, 61 U.S.P.Q.2d 1430, 1435 (Fed. Cir. 2001). Thus claim 11 is patentable, and the rejection should be reversed as to claim 11 and claims 13, 16-18, 20, 44 and 45 depending therefrom.

B. Claim 12 Is Patentable Under 35 U.S.C. §103(a) Over Shay in View of Ansel

Claim 12 depends from claim 11 and further recites that the integrated circuit includes a logic functionality to emulate logic that is difficult to trigger and to determine whether the supply voltage has reached a level sufficient to trigger the difficult to trigger logic. Claim 12 stands rejected under 35 U.S.C. §103(a) over Shay in view of U.S. Patent No. 5,809,312 ("Ansel"). The rejection is improper.

The Examiner concedes that Shay does not teach or suggest such logic functionality. Nor does Ansel teach or suggest the claimed logic functionality. In this regard, while Ansel discloses certain logic, nowhere does Ansel teach or suggest that this logic emulates logic that is difficult to trigger. Instead, Ansel merely discloses logic that emulates certain critical circuits of an integrated circuit. Thus in addition to the reasons discussed above regarding claim 11, the rejection of claim 12 is improper for this further reason, and should be reversed.

C. Claim 46 Is Patentable Under 35 U.S.C. §103(a) Over Shay in View of Wu

Dependent claim 46 depends from claim 17 and recites that a capacitor circuit includes a first capacitor coupled to a supply voltage and a second capacitor coupled to the first capacitor through a transistor. More so, claim 17 (from which claim 46 depends) recites that the capacitor circuit enables the supply voltage to reach a designated output level. Claim 46 stands rejected under 35 U.S.C. §103 over Shay in view of U.S. Patent No. 6,288,584 ("Wu"). This rejection is improper.

While Wu discloses capacitors, nowhere does Wu teach or suggest that such capacitors may be used to enable a supply voltage to reach a designated output level. Nor is there any motivation to combine the capacitor structure of Wu with the circuit of Shay. Claim 46 is further patentable for the same reasons discussed above with regard to claim 11. For at least these reasons, the rejection is improper and should be reversed.

IX. CONCLUSION

Since the rejections of the claims are baseless, they should be reversed.

Respectfully submitted,

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APPENDIX OF CLAIMS

The claims on appeal are:

11. An integrated circuit comprising:

an activation circuit to determine whether a supply voltage reaches a predetermined level, said activation circuit including an inverter coupled to the gate of a load transistor, a second transistor coupled to said load transistor and a third transistor coupled between said load transistor and said second transistor;

a pulse generator to generate pulses to indicate that the supply voltage is ramping up and to terminate the generation of the pulses after the supply voltage reaches a predetermined level; and

a feedback path to provide an output of said pulse generator to said activation circuit, the activation circuit to latch a high signal in response to a low signal on said feedback path.

12. The integrated circuit of claim 11 further including a logic functionality to emulate logic that is difficult to trigger and to determine whether the supply voltage has reached a level sufficient to trigger the difficult to trigger logic.

13. The integrated circuit of claim 11 including a level detector that detects when a voltage is above at least two transistor threshold voltages, said level detector operative to control said pulse generator.

16. The integrated circuit of claim 11 including a pair of transistors that must both conduct in order to generate said pulses.

17. The integrated circuit of claim 16 including a capacitor circuit to enable the supply voltage to reach a designated output level.

18. The integrated circuit of claim 17 including a hysteresis sense stage coupled to said capacitor circuit.

20. The integrated circuit of claim 11 including a circuit to latch the pulse generator in response to the supply voltage being in a first state.

44. The integrated circuit of claim 11 wherein the load transistor is coupled to the supply voltage.

45. The integrated circuit of claim 11 further including a second activation circuit to determine whether the supply voltage reaches the predetermined level.

46. The integrated circuit of claim 17 wherein the capacitor circuit includes a first capacitor coupled to the supply voltage and a second capacitor coupled to the first capacitor through a transistor.